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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,573	07/24/2003	Masatoshi Sakamoto	HITA.0415	7728

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EXAMINER	
NGUYEN, VAN THU T	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 11/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,573	SAKAMOTO ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/21/2005 - Amendment*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *4-9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. Acknowledgement is made for Amendment filed on January 21, 2005.

2. Claims 1-9 are pending.

3. Claims 1-3 are still present for examination.

4. Claims 4-9 are withdrawn from consideration.

Response to Arguments

5. Applicant's arguments filed January 21, 2005 have been fully considered but they are not persuasive.

(a) Applicants argue that, in the present invention, a write operation is being executed at the same time as a read operation based on FIGS. 4-5 and Specification, "*the column selection switch for read is turned ON even during the write operation*", page 2, lines 12-14, and "*the Y selection line WYS for write to control the operation of the column selection switch in the write amplifier is isolated from the Y selection line RYS for read to control the operation of the column selection switch in the read amplifier*", page 6, lines 10-12. However, Applicants have misinterpreted the Specification for the following reasons:

(1) Specification, page 2, line 5 to page 4, line 8, does not disclose the invention itself. Instead, it presents a disadvantage of related art, which is when "*the column selection switch for read is turned ON even during the write operation, the through-current flows in some cases between a precharge circuit of the read IO line and a read amplifier, and thereby power consumption is*

increased", page 2, lines 12-17. Therefore, "*an object of the present invention is to provide a technical means to reduce a through-current*", page 4, lines 9-10.

(2) The phrase "*the column selection switch for read is turned ON even during the write operation*" is not equivalent to a write operation is being executed at the same time as a read operation. According to Specification, page 2, lines 12-17, that is what happens when column selection switch for write and column selection switch for read are controlled with the common control line.

(3) FIGS. 4-5 do not show a write operation is being executed at the same time as a read operation. FIG. 4 shows an operation timing diagram in the read operation of the DRAM, where column selection signal RYS is on/off for transferring data from the bit lines while column selection signal WYS is maintaining off during the cycle. FIG. 5 shows an operation timing diagram in the write operation of the DRAM, where the column selection signal WYS is on/off for transferring data to the bit lines, while column selection signal RYS is maintaining off during the cycle. There is no indication in FIGS. 4-5 that the write operation is being executed at the same time as the read operation.

(4) The phrase "*the Y selection line WYS for write to control the operation of the column selection switch in the write amplifier is isolated from the Y selection line RYS for read to control the operation of the column selection switch in the read amplifier*" is not equivalent to Y/column address of a read operation is different from the Y/column address of a write operation. It only means the that

column selection switch WYS for write and column selection switch RYS for read operation [of the same column] are controlled in different timing.

(b) As understood, Applicants argue that Naritake does not disclose a read operation and a write operation performed simultaneously, however, it is noted that such feature are not recited in the rejected claim(s).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-2 are rejected under 35 U.S.C. 102(a)/102(e) as being anticipated by Naritake (U.S. Patent No. 6,339,560).

Regarding claim 1, Naritake discloses, in FIG. 2, a semiconductor memory device comprising:

a write signal line (short lines connected between M12-M13 to DLn-/DLn) to transmit write data;

a write column selection switch (M12-M15) being possible to transmit said write data on said write signal line to a bit line (BL0n and /BL0n);

a write column selection line (WS0) supplying an operation control signal to said write column selection switch;

a sense amplifier column comprising a plurality of sense amplifier circuits (plurality of SA) to amplify read data which are read to said bit line from a memory cell;

a read signal line (short lines connected between M8-M9 to DLn-/DLn) to transmit read data, said read signal line being different from said write signal line;

a read column selection switch (M8-M11) to selectively transmit the read data of said bit line to said read signal line;

a read column selection line (RS0) supplying an operation control signal to said read column selection switch; and

an inherent control circuit to control operations of said write column selection switch and read column selection switch in different timings (see WS0 and RS0 signals in FIG. 8);

wherein said write signal line and said read signal line are allocated crossing said sense amplifier column and said write column selection line and said read column selection line are allocated in parallel to said sense amplifier column (DLn and /DLn crossing the column formed by plurality of SA, RS0 and WS0 in parallel to the column formed by plurality of SA, see FIG. 2).

Regarding claim 2, Naritake further discloses, in FIG. 2, wherein said sense amplifier circuit comprises a write amplifier section (comprising of M12-M15) to drive said bit line based on the data of said write signal line and a read amplifier section (comprising of M8-M11) to drive said read signal line based on the data of said bit line, wherein said write column selection line is provided using a wiring layer in the area where said write amplifier section is formed (34),

and wherein said read column selection line is provided using a wiring layer in the area where said read amplifier section is formed (33).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Naritake in view of Yamada et al. (U.S. Patent No. 5,506,808).

Regarding claim 3, Naritake discloses, as applied in prior rejection of claims 1-2, all claimed subject matter except further limitation as in claim 3.

Yamada et al. disclose, in FIG. 12, sense amplifier circuit comprising of a write amplifier section (3), a sense amplifier section (4), and a read amplifier section (output circuit 5) in order from left to right.

Since Naritake and Yamada et al. are both from the same field of endeavor, the purpose disclosed by Yamada et al. would have been recognized in the pertinent art of Naritake.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to have the write amplifier section, the sense amplifier section, and the read amplifier section of the sense amplifier circuit in order listed because it has been held that re-arranging parts of an invention involves only routine skill in the art.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 17, 2005

VanThu Nguyen
Primary Examiner
Art Unit 2824